



SILICON SOFTWARE

microEnable III

microEnable III XXL

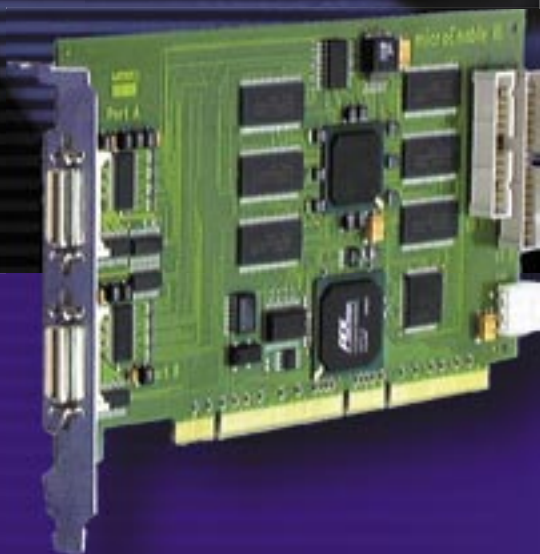
Availability of a new **high resource performance model**

High data transfer over **PCI 64-bit/66 MHz** interface

Integrated real time **image preprocessing** features

Programming of **individual functionality**

Support of multiple **operation systems**



... try individuality

microEnable III

microEnable III-XXL

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Benchmarks

- camera frequency up to 85 MHz clock rate
- area cameras up to 8K*4K pixels
- line cameras up to 16K pixels/line
- over 200 MByte/s continuous data transfer rate to user-memory
- framerates more than 10.000 f/s
- all multi-tap modes
- synchronous operation of two cameras in dual camera mode
- independent operation and control of cameras
- support of multiple sensor read-out formats
- asynchronous image acquiring in triggered mode
- seperated framebuffers

Preprocessing features

- real time 3x3 Bayer filter
- variable sensor read-out
- white balancing
- 2D shading correction
- CMOS fixed pattern noise suppression
- 1D shading correction (line cameras)
- 10 to 8 look-up table (LUT)

Customized preprocessing features

- customized image preprocessing on demand
- VisualApplets Studio
Base version with ability to configure and recompile the delivered applets and use additional image preprocessing functions from a vision library (available Q2/04)
- VisualApplets Studio
Extended version with ability to program individual vision algorithms and preprocessing functions by VHDL import or a C++ based FPGA programming tool (avail.Q2/04)

Software features

- software development kit (SDK)
- hardware diagnostic tool
- monitoring program microDisplay

Additional interfaces

- TTL trigger interface with 8 / 4 IOs

Supported OS

- Windows NT 4.0, Windows 2000, Windows XP
- Linux
- Real time Linux (RTAI)
- QNX

comparison table

	standard	XXL
vision processor		
Xilinx FPGA	XC2S 300 E	XC2S 600 E
preproc. resources	high	very high
hardware equipment		
PC host interface	PCI 64-bit / 66 MHz	
on-board memory	96 MBytes	
camera interfaces	2 CameraLink inputs	
digital interfaces	trigger connector	
applets for Area cameras		
BASE config.	Single Gray	Single Gray
	Single Bayer	Single Bayer
	Single RGB	Single RGB
	Dual Gray	Dual Gray
	Dual RGB	Dual RGB
	n/a	Dual Bayer
MEDIUM config.	n/a	Area Gray*
	n/a	Area RGB*
applets for Line cameras		
BASE config.	Single Gray	Single Gray
	Single RGB	Single RGB
	Dual Gray	Dual Gray
	Dual RGB	Dual RGB
MEDIUM config.	n/a	Line Gray*

* available soon



Technical feature

Hardware features

- intelligent framegrabber with vision processor
- Xilinx Spartan 2 - FPGA processor
- PCI 64-bit / 66 MHz interface
- 96 MB SDRAM memory

General features

- exploitation of the complete physical memory
- multiprocessor capability
- multi PCI-bus capability (only limited by numbers of available PCI-busses)
- programming of individual solutions by direct access to FPGA-coprocessor

CameraLink features

- 2 x CameraLink interfaces
- 2 x BASE or 1 x MEDIUM configuration

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